OVERVIEW

Packet Generator is a software tool that will be running on a Host computer and generate traffic patterns.

AHB packet generator is a product that as a Master generates series of AHB Read and Write transactions which can be used by emulator platform to generate traffic on DUT Slave's interfaces. Also it can be used on Simulation platform to generate traffic on simulation environment on DUTs interface.

AHB is a new generation of AMBA bus which is intended to address the requirements of high-performance synthesizable designs. AMBA AHB is a new level of bus which sits above the APB and implements the features required for high-performance, high clock frequency systems including:

- burst transfers
- split transactions
- single cycle bus master handover
- single clock edge operation
- non-tristate implementation
- wider data bus configurations (64/128 bits).

An AMBA-based microcontroller typically consists of a high-performance system backbone bus, able to sustain the external memory bandwidth, on which the CPU and other Direct Memory Access (DMA) devices reside, plus a bridge to a narrower APB bus on which the lower bandwidth peripheral devices are located. Figure 1 shows both AHB and APB in a typical AMBA system.

Tools & Technologies: Verilog, SystemVerilog, C, DPI, UVM
EDA Tools
Emulators

BENEFITS
• These methods can be used for verification of most complex hardware design to simple hardware design
• Easy to use solution, plug and play type solutions
• Software packet generators are very cost-effective solutions, they are cheaper compared to high license costing software products available in the market.
• Creates beautiful Emulation environment, which can mimic many simulation verification scenarios.
• Detect bug in Pre-silicon phase, which can save millions of dollars of re-spinning silicon cost.
• Post-silicon also software portion can be used for validation
• Help to build a parallel structure to simulation to find more design bugs quickly.
• The overall runtime can be reduced to as much as 10 times than long SOC simulations. This can speed up TAPE OUT of the chip.
• Scoreboarding and traffic analysis can be done very well in the Software solution.

FEATURES

- It works on two types of configuration modes: AHB Read and AHB Write.
- The physical AHB bus which transfers the generated data mainly consists of below signals. All signals are prefixed with the letter **H**, ensuring that the AHB signals are differentiated from other similarly named signals in a system design.
  - HCLK
  - HWRITE
  - HWDATA
  - HRESETn
  - HSIZE
  - HRDATA
  - HADDR
  - HBURST
  - HTRANS
  - HPROT

  The AMBA AHB bus protocol is designed to be used with a central multiplexor interconnection scheme. Using this scheme all bus masters drive out the address and control signals indicating the transfer they wish to perform and the arbiter determines which master has its address and control signals routed to all of the slaves. A central decoder is also required to control the read data and response signal multiplexor, which selects the appropriate signals from the slave that is involved in the transfer.
- An AHB bus master has the most complex bus interface in an AMBA system. Typically an AMBA system designer would use predesigned bus masters and therefore would not need to be concerned with the detail of the bus master interface.
- An AHB bus slave responds to transfers initiated by bus masters within the system. The slave uses a HSELx select signal from the decoder to determine when it should respond to a bus transfer. All other signals required for the transfer, such as the address and control information, will be generated by the bus master.
- The role of the arbiter in an AMBA system is to control which master has access to the bus. Every bus master has a REQUEST/GRANT interface to the arbiter and the arbiter uses a prioritization scheme to decide which bus master is currently the highest priority master requesting the bus.
- Each master also generates a HLOCKx signal which is used to indicate that the master requires exclusive access to the bus.
- The decoder in an AMBA system is used to perform a centralized address decoding function, which improves the portability of peripherals, by making them independent of the system memory map.

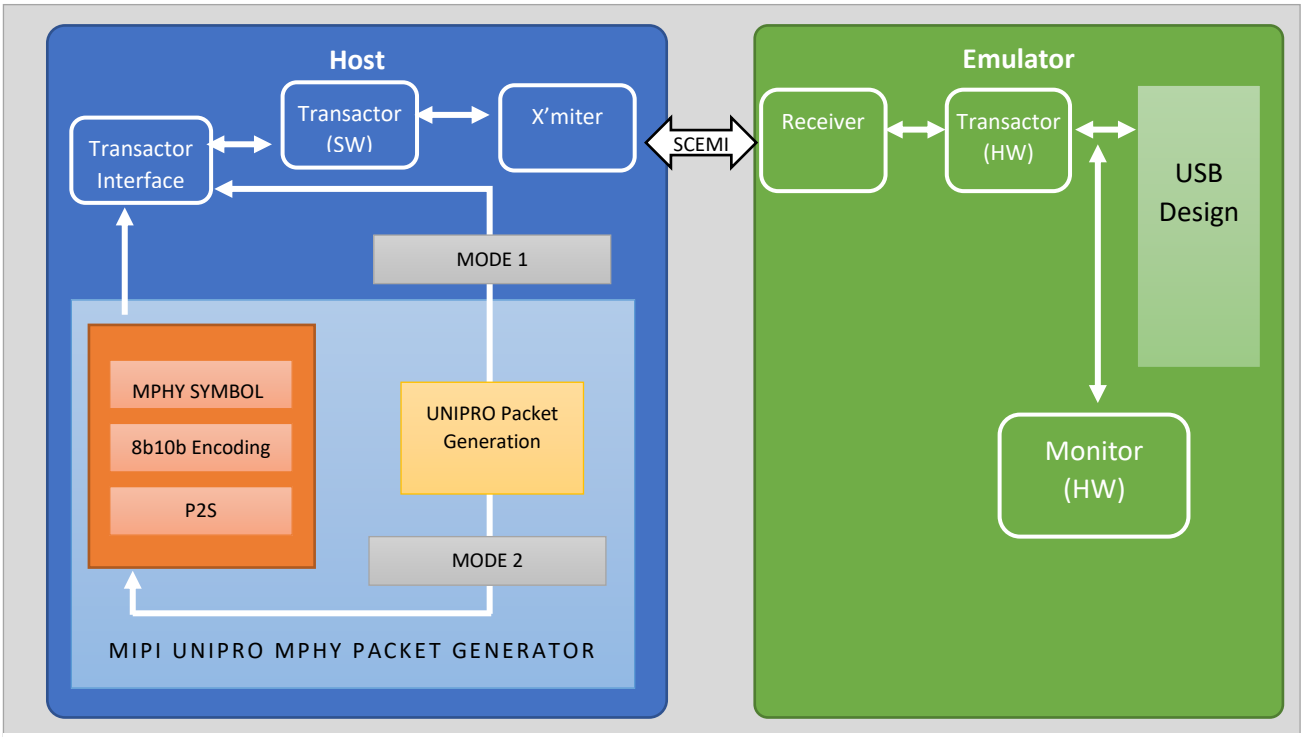

Figure 1: MIPI UNIPRO MPHY in EMULATION PLATFORM

MIPI UNIPRO PACKET

MIPI UNIPRO PACKET comprises of all types of MIPI Unipro PHY-Adaptor Symbols.
MIPI Unipro PHY-Adaptor Layer (Layer L1.5) generates PA Symbol. This PA Symbol can be categorized into two main types

- **Data Symbol**
  It is a 17-bit symbol, where 16-bit is always 0.

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Data															

Figure 2: Data Symbol

- **Control Symbol**
  It is a 17-bit symbol, where 16-bit is always 1.
  This control symbol is divided into two parts, EscType field (bits [15:8]) and EscParam (bits [7:0]).
  EscType shall be set to ESC_PA(11111110).
  For Peer to Peer communication PACP Frames are used.
  PACP is a control frame.

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	EscType								EscParam							

Figure 3: Control Symbol

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	ESC_PA								EscParam_PA = PACP_BEGIN							
0	PACP_FunctionId															
0	Parameters															
0	...															
0	CCITT CRC-16															

Figure 4: PACP Control Frame

MIPI UNIPRO-MPHY PACKET

MIPI UNIPRO-MPHY Packet generation logic is based on MPHY state machine, where at every state MPHY compliant control symbols are generated. These control symbols act as start of frame symbol for received Unipro symbol and end of frame symbol for received Unipro Symbol.

Features of Unipro MPHY Packet Generations:

- Receives Data from Phy-Adaptor Layer of Unipro
- Convert Parallel Data to serial Data
- Convert 8 bit of data to 10 bit of data using 8b-10b encoder
- Send 10 bit of data along with start of frame symbol as Marker0(MK0) and end of frame as MK2.

These MPHY Control Symbols are:

- FILLER
- MK0
- MK2
- MK2