OVERVIEW

Packet Generator is a software tool that will be running on a Host computer and generate traffic patterns. DDR packet generator is a product that generates series of Write and Read commands, which can be used by emulator platform to generate traffic on DUTs interfaces. It can also be used on Simulation platform to generate traffic on simulation environment on DUTs interface.

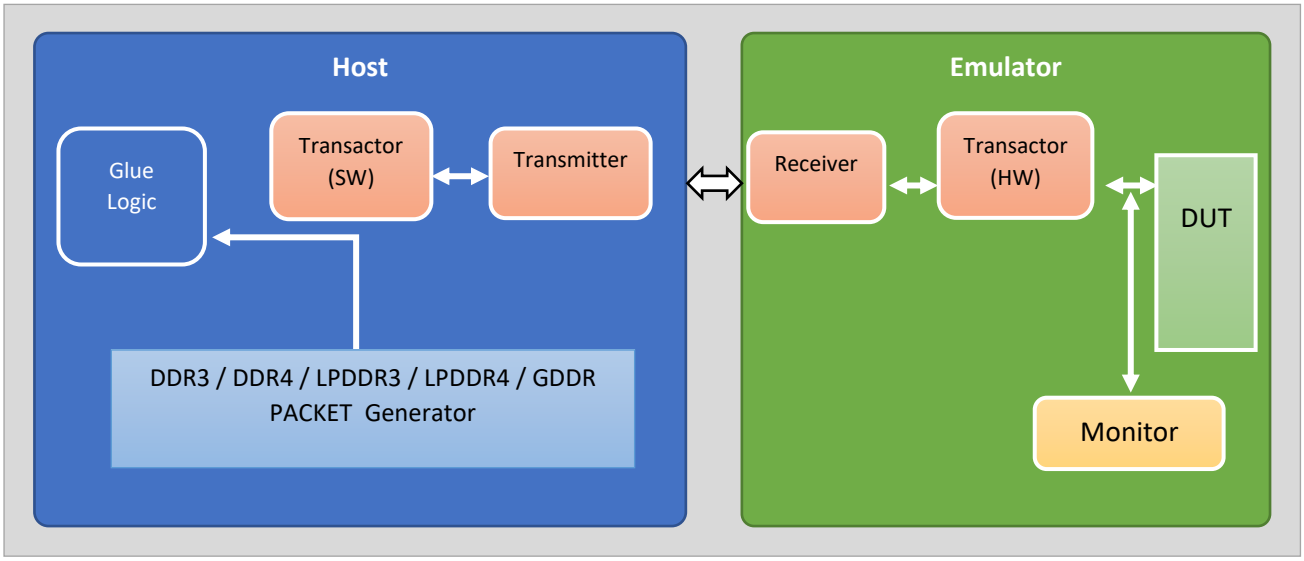

Figure 1: DDR PACKET GENERATOR in EMULATION PLATFORM

FEATURES

- It works two type of configuration modes:
  Write and Read
- All DDR Packet generation logic can support different DDR memory types like
  - DDR3
  - LPDDR3
  - DDR4
  - LPDDR4
  - GDDR
- The key aspects:
  - Different Speed bins
  - Different RANK structures
  - Configurable addressing modes
  - RMW support
- Supports different speed bins
  - 1066
  - 1600
  - 1866
  - 2133
  - 2400
  - 3200
  - 3733
  - 4266
- Command supports

BENEFITS
• These methods can be used for verification of most complex hardware design to simple hardware design
• Easy to use solution, plug and play type solutions
• Software packet generators are very cost-effective solutions, they are cheaper compared to high license costing software products available in the market.
• Creates beautiful Emulation environment, which can mimic many simulation verification scenarios.
• Detect bug in Pre-silicon phase, which can save millions of dollars of re-spinning silicon cost.
• Post-silicon also software portion can be used for validation
• Help to build a parallel structure to simulation to find more design bugs quickly.
• The overall runtime can be reduced to as much as 10 times than long SOC simulations. This can speed up TAPE OUT of the chip.
• Scoreboarding and traffic analysis can be done very well in the Software solution.

Function	Abbreviation	CKE		CS_n	ACT_n	RAS_n /A16	CAS_n /A15	WE_n/ A14	BG0-BG1	BA0-BA1	C2-C0	A12/ BC_n	A17, A13, A11	A10/ AP	A0-A9
		Previous Cycle	Current Cycle												
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code			
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X
				L	H	H	H	H	V	V	V	V	V	V	V
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V
RFU	RFU	H	H	L	H	L	H	H	RFU						
Bank Activate	ACT	H	H	L	L	Row Address (RA)			BG	BA	V	Row Address (RA)			
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V

CONFIGURATIONS

There are different address configurations possible:

- 2GB Addressing Table
- 4GB Addressing Table
- 8GB Addressing Table
- 16GB Addressing Table

Tools & Technologies: Verilog, SystemVerilog, C, DPI, UVM
EDA Tools
Emulators