OVERVIEW

Packet Generator is a software tool that will be running on a Host computer and generate traffic patterns. Ethernet packet generator is a product that generates series of Packets which can be used by emulator platform to generate traffic on DUTs interfaces. Also, it can be used on Simulation platform to generate traffic on simulation environment on DUTs interface. Packet Generator allows us to create and send any possible packet or sequence of packet on Ethernet link.

FEATURES

- Ethernet Traffic generator supports complete range of copper and optical Gigabit Ethernet and 10/40/100-Gigabit Ethernet modules and provides consumer the emulation of Ethernet protocol with PHY layer.
- Frame formats: DIX, IEEE 802.3, IEEE 802.1Q, IEEE 802.1ad/Q-in-Q
- Ethernet Traffic Generator support these PHY interfaces:
    - SFP: 10BASE-T, 100BASE-TX, 100BASE-FX, 1000BASE-T, 1000BASE-SX, 1000BASE-LX, 1000BASE-ZX
    - RJ-45: 10BASE-T, 100BASE-TX, 1000BASE-T
    - On/off laser control for optical interfaces
- Manual and Auto-Negotiated Link Speeds.
    - Rate negotiation: 10/100/1,000Mbps
- Support for Jumbo frames.
- Ethernet Traffic Generator also supports Layer4 and Layer3 fully configurable packets.
    - Transport Layer Protocol: UDP, TCP.
    - Network Lauer Protocol: IPv4, IPv6.
- MPLS generation and analysis
- Insertion of FCS error and undersized frames.
- It can Send sequence of packets with
    - Number of packets
    - Delay between packets
    - Configured speed Rate

- Parameter values change like change IP & Mac address, UDP payload, 2 user defined bytes, etc.
- Configured Burst

BENEFITS

- These methods can be used for verification of most complex hardware design to simple hardware design
- Easy to use solution, plug and play type solutions
- Software packet generators are very cost-effective solutions, they are cheaper compared to high license costing software products available in the market.
- Creates beautiful Emulation environment, which can mimic many simulation verification scenarios.
- Detect bug in Pre-silicon phase, which can save millions of dollars of re-spinning silicon cost.
- Post-silicon also software portion can be used for validation
- Help to build a parallel structure to simulation to find more design bugs quickly.
- The overall runtime can be reduced to as much as 10 times than long SOC simulations. This can speed up TAPE OUT of the chip.
- Scoreboarding and traffic analysis can be done very well in the Software solution.

CONFIGURATIONS

There are five types of Ethernet frame:

- The Ethernet Version 2 or Ethernet II frame, the so-called DIX frame (named after DEC, Intel, and Xerox
- Raw 802.3 frame without LLC
- IEEE 802.x LLC frame
- IEEE 802.x LLC/SNAP frame
- Ethernet Jumbo frame

Speed Rate of Ethernet Frames:

- The Standards Speed Ethernet
    - 10Mbps and 100Mbps
- Gigabit Ethernet
    - 100Mbps up to 1000Mbps and 10Gbps
- 25G/40G/100G/400G Ethernet

Tools & Technologies: Verilog, SystemVerilog, C, DPI, UVM
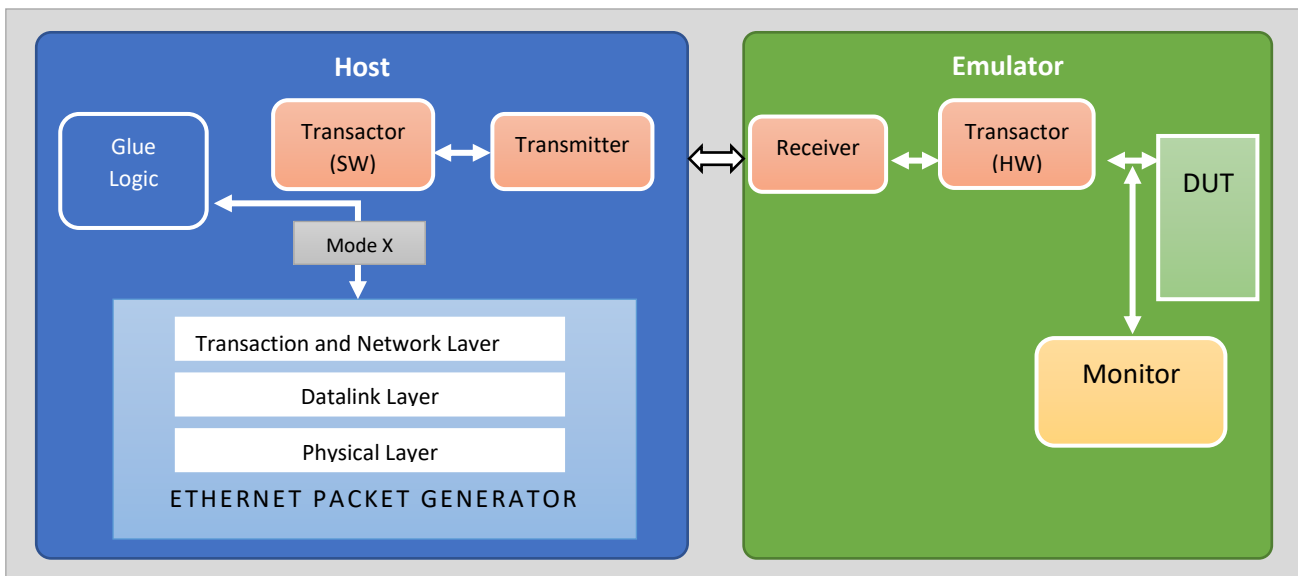EDA Tools
Emulators

Figure 1: Ethernet PACKET GENERATOR in EMULATION PLATFORM

- Physical Ethernet Packet Looks like:

Figure 2 Ethernet Frame Structure

- Preamble
    - This is a stream of bits used to allow the transmitter and receiver to synchronize their communication. The preamble is an alternating pattern of binary 56 ones and zeroes
- Start Frame Delimter
    - This is always 10101011 and is used to indicate the beginning of the frame information.
- Destination MAC
    - This is the MAC address of the machine receiving data.
- Source MAC
    - This is the MAC address of the machine transmitting data.
- Length
    - This is the length of the entire Ethernet frame in bytes. Although this field can hold any value between 0 and 65,534, it is rarely larger than 1500 as that is usually the maximum transmission frame size for most serial connections.
- Data/Padding (a.k.a. Payload)
    - The data is inserted here. This is where the IP header and data is placed if you are running IP over Ethernet. This field contains IPX information if you are running IPX/SPX (Novell). Contained within the data/padding section of an IEEE 803.2 frame are four specific fields:
- DSAP - Destination Service Access Point
    SSAP - Source Service Access Poiont
    CTRL - Control bits for Ethernet communication
    NLI - Network Layer Interface
- FCS
    - This field contains the Frame Check Sequence (FCS) which is calculated using a Cyclic Redundancy Check(CRC). The FCS allows Ethernet to detect errors in the Ethernet frame and reject the frame if it appears damaged.