OVERVIEW

NVM Express is a scalable host controller interface designed to address the needs of Enterprise, Data Center and Client systems for supporting chip-to-chip, board-to-board, adapter and distance solutions as shown in Figure 1. The protocol can efficiently use interconnect and fabric technologies such as PCI Express, Ethernet and Fiber Channel. This product provides traffic generator, protocol analysis, emulation, exerciser and other test equipment to service all NVMe storage applications.

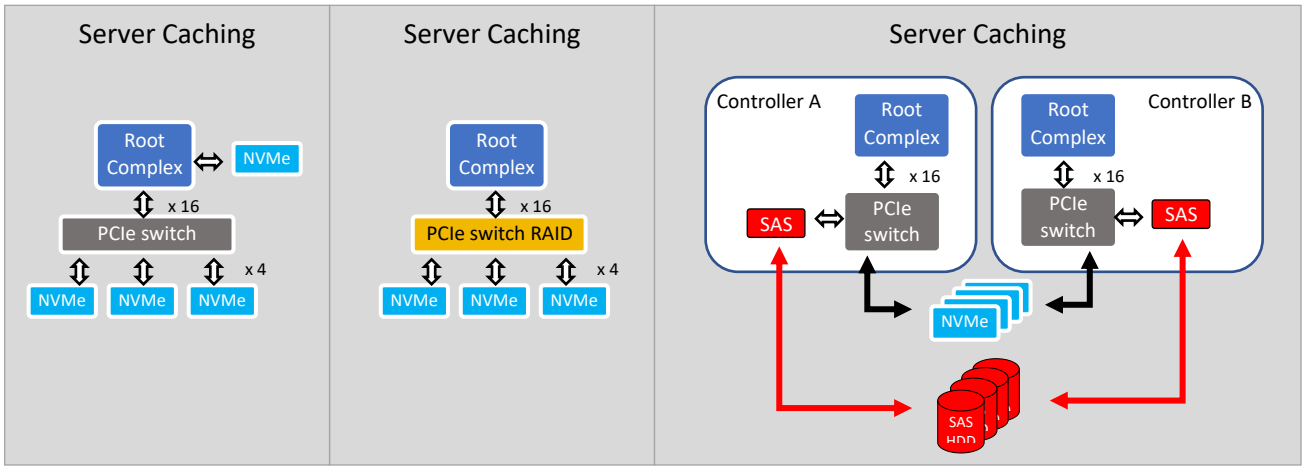

Figure 1: ONFI PACKET GENERATOR in EMULATION PLATFORM

As storage developers make the transition from legacy SAS and SATA protocol-based SSDs to the more advanced NVMe and SATA Express technologies, they are encountering limitations in available design and test tools including limited trace recording times and a lack of standardized analysis reports for PCIe-based storage.

These two issues are significant for the newer technologies of NVMe and SATA Express due to the following

- High performance SSD testing can require recording data traffic beyond a few minutes. This is not possible for many protocol analyzers due to limitations in their recording architectures.

While some test tool suppliers have claimed support for the NVMe and SATA Express protocols, support for these protocols has remained minimal. This has hampered developer's productivity due to the use of reporting systems designed for the older technologies, which are not optimized for quality testing on NVMe and SATA Express products.

Developers of SSDs that utilize NVM Express face challenging testing, problem identification and resolution issues that must be solved quickly to maintain project schedules. This product understands and decode these specifications, in addition to all standard PCIe traffic.

An NVMe controller is associated with a single PCI function. The capabilities and settings that apply to the entire controller are indicated in a controller capabilities (CAP) register and an identify controller data structure.

NVMe is based on paired submission and completion queue mechanism (Figure 2). Command are placed by host software into submission queue. Completions are placed into the associated completion queue by the controller. Multiple submission queue may utilize same completion queue. Submission and completion queue are allocated in memory.

BENEFITS
• These methods can be used for verification of most complex hardware design to simple hardware design
• Easy to use solution, plug and play type solutions
• Software packet generators are very cost-effective solutions, they are cheaper compared to high license costing software products available in the market.
• Creates beautiful Emulation environment, which can mimic many simulation verification scenarios.
• Detect bug in Pre-silicon phase, which can save millions of dollars of re-spinning silicon cost.
• Post-silicon also software portion can be used for validation
• Help to build a parallel structure to simulation to find more design bugs quickly.
• The overall runtime can be reduced to as much as 10 times than long SOC simulations. This can speed up TAPE OUT of the chip.
• Scoreboarding and traffic analysis can be done very well in the Software solution.

An admin submission and the associated completion queue exists for the purpose of controller management and control (e.g. Creation and deletion of I/O submission and completion queues, aborting commands, etc.). Only commands that are part of admin command set may be submitted to the admin submission queue. The interface provides optimized command submission and completion paths. It includes support for parallel operation by supporting up to 65,535 I/O queues with up to 64K outstanding commands per I/O queue

Some of the main features of NVMe are:

- No requirement for un-cacheable/MMIO register reads in the command submission or completion path.
- A maximum of 1 MMIO register write is necessary for the command submission path.
- Support for up to 65536 I/O queues, with each I/O supporting up to 64K outstanding commands.
- Priority associated with each I/O queue with a well-defined arbitration mechanism.
- All information to complete a 4KB read request is included in the 64B command itself, ensuring efficient small I/O operation
- An official and streamlined command set.
- Support for MSI/MSI-X and interrupt aggregation.
- Efficient support for I/O virtualization architectures, such as SR-IOV.
- Robust error reporting and management capabilities.
- Support for multi-path I/O and namespace sharing

KEY FEATURES

NVMe traffic generator, protocol analyzers and exercisers are needed to be developed for SSD and other similar storage products using the new NVMe, SATA Express and SCSI Express high-speed serial data standards. Traffic generator, protocol analyzers and exercisers are used by developers and validation engineers to directly send data via emulator, record and examine data traffic on serial data communication links between devices and systems. This equipment enables developers to reduce debug and test schedules, lower engineering development costs on new products and meet aggressive time-to-market requirements.

NVMe Traffic Generator is a software tool that will be running on a Host computer via emulator and will generate complex, random and extensive test scenario packets as per NVMe protocol.

1. Plug and play

In order to make the NVMe traffic generator work out-of-the-box and easier to deploy, a number of integration kits are available for some commonly used PCIe design IP. The kits are basically a reference resource to enable the smooth integration of DUTs with UVM testbenches for running first stimulus.
Also, single and multiple NVMe controller use-case examples are part of the standard deliverable database.

2. In-depth protocol feature support

NVMe traffic generator provides extensive protocol feature support to allow for a wider degree of stimuli generation. Some of the supported features are:

- Multipath IO and namespace sharing.
- Configurable queue depth, number and n:1 queue pairing.
- Pin, MSI, and MSI-X interrupts with/without masking.
- Complete admin and NVMe command set.
- PRP and scatter gather lists.
- Non-contiguous queue operations.
- Metadata as extended LBA or separate buffer.
- Namespace management.
- End-to-end protection.
- Security and reservations.
- Host memory buffer.
- Enhanced status reporting.
- Controller memory buffer

3. Multiple controller support

NVMe traffic generator supports multiple controller operations. Since each single root I/O virtualization (SR-IOV) PCIe physical or virtual function can act as an NVMe controller, NVMe traffic generator as a host can generate stimuli on the target controller or respond as a controller based on its location in the bus topology (bus, device, function number).

4. API based stimuli

NVMe traffic generator provides a rich set of APIs for easier stimuli generation. These APIs can be categorized as transactional, attribute/command-specific, and utility-based. They provide a simple interface to initiate traffic from a higher level of abstraction (transactional) or precise control at the command (command-specific) or byte levels. Users can modify stimulus at the byte-abstraction level for intentional error injection.

Conclusion

NVMe is designed to optimize the processor's driver stack so it can handle the high IOPS associated with flash storage. It also puts the SSD close to the server chipset, reducing latency and further increasing performance while keeping the traditional form factor that IT managers are comfortable servicing. It brings PCIe SSDs into the mainstream with a streamlined protocol that is efficient, scalable and easy-to-deploy thanks to industry standard support. NVMe traffic generator perfectly complements verification engineering efforts for timely design closure by providing easy stimuli generation and debugging interfaces, so teams can focus more on protocol-level intricacies.

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