OVERVIEW

ONFi specification defines a standardized NAND Flash device interface that provides the means for a system to be designed that supports a range of NAND Flash devices without direct design pre-association. The solution also provides the means for a system to seamlessly make use of new NAND devices that may not have existed at the time that the system was designed.

Packet Generator is a software tool that will be running on a Host computer and generate traffic patterns.

ONFI packet generator is a product that generates series of NAND Flash interface compliant packet which can be used by emulator platform to generate traffic on DUTs interfaces. It can also be used on Simulation platform to generate traffic on simulation environment on DUTs interface.

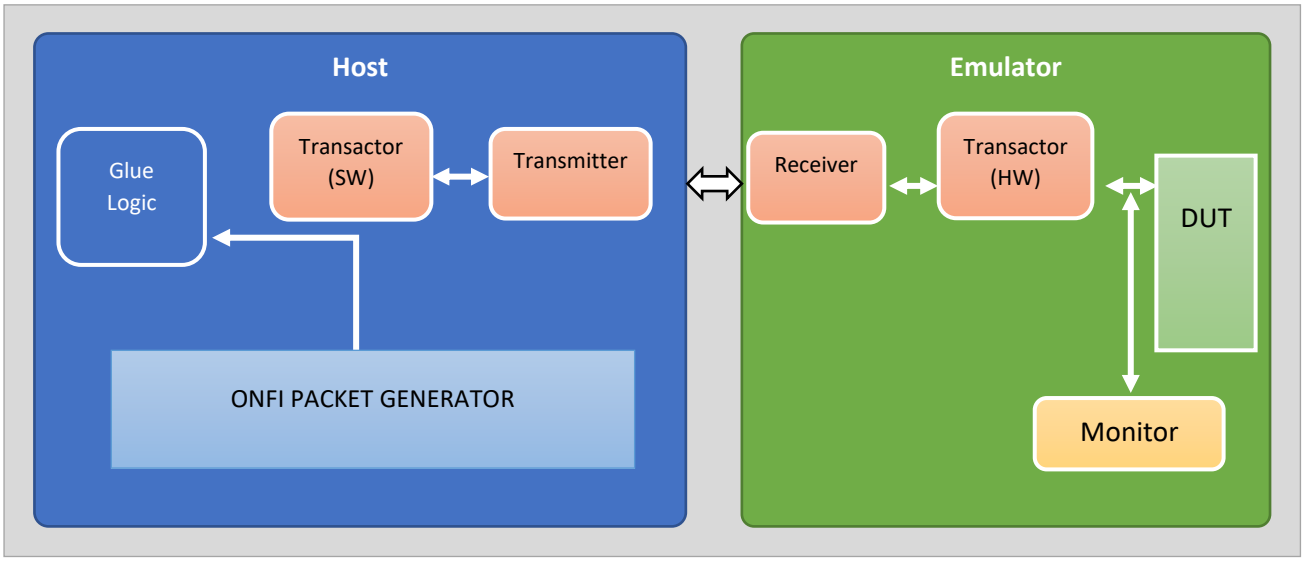

Figure 1: ONFI PACKET GENERATOR in EMULATION PLATFORM

GOALS & REQUIREMENTS

- Support range of device capabilities and new unforeseen innovation
- Consistent with existing NAND Flash designs providing orderly transition to ONFI
- Capabilities and features are self-described in a parameter page such that hard-coded chip ID tables in the host are not necessary
- Flash devices are interoperable and do not require host changes to support a new Flash device
- Define a higher speed NAND interface that is compatible with existing NAND Flash interface
- Allow for separate core (Vcc) and I/O (VccQ) power rails
- Support for offloading NAND lithography specific functionality to a controller stacked in the NAND package (EZ NAND)

BENEFITS
• These methods can be used for verification of most complex hardware design to simple hardware design
• Easy to use solution, plug and play type solutions
• Software packet generators are very cost-effective solutions, they are cheaper compared to high license costing software products available in the market.
• Creates beautiful Emulation environment, which can mimic many simulation verification scenarios.
• Detect bug in Pre-silicon phase, which can save millions of dollars of re-spinning silicon cost.
• Post-silicon also software portion can be used for validation
• Help to build a parallel structure to simulation to find more design bugs quickly.
• The overall runtime can be reduced to as much as 10 times than long SOC simulations. This can speed up TAPE OUT of the chip.
• Scoreboarding and traffic analysis can be done very well in the Software solution.

PerfectVIPs

ONFI PACKET GENERATOR

DATASHEET

FEATURES

- ONFI supports four different data interface types: SDR, NV-DDR, NV-DDR2, and NV-DDR3.
- The SDR data interface is the traditional NAND interface that uses RE_n to latch data read, WE_n to latch data written, and does not include a clock.
- The NV-DDR data interface is double data rate (DDR), includes a clock that indicates where commands and addresses should be latched, and a data strobe that indicates where data should be latched.
- The NV-DDR2 data interface is double data rate (DDR) and includes additional capabilities for scaling speed like on-die termination and differential signaling.
- The NV-DDR3 data interface includes all NV-DDR2 features but operates at VccQ=1.2V
- ONFi Packet generation logic generates command specific (Chapter 5.1 – ONFI command set) fields such as row address, column address, command opcode and data.
- ONFi Packet generation logic generates command specific functionality on a bi-directional interface which can be used at emulation platform or at simulation platform.
- Chapter-4 of ONFi protocol defines the interface timing diagrams for Input, output, configuration & status respective to each interface mode (SDR, NV-DDR, NV-DDR2, and NV-DDR3).

ONFI PACKET

ONFI PACKET comprises of all Command types of ONFI transaction fields.

- **DATA INTERFACE COMPARISON**
- **SIGNAL ASSIGNMENT BASED ON DATA INTERFACE TYPE**

ONFI Packet generation logic is based on command set; where at every command compliant control fields are generated.

A write packet fields framed as:

- Target address on which target command has to operate
- Command enum which defines the PAGE PROGRAM command set (‘h80 – ‘h10)
- Row address which specifies LUN, BLOCK(PLANE) & PAGE address
- Column address which specifies the start address location inside the page
- End transaction specifies whether the PROGRAM operation ends or extended for random data input commands
- Data size which defines the size of the data needs to be programmed.
- Data filed which sets the what kind of random data/packet data requires to be programmed

A read packet fields framed as:

- Target address on which target command has to operate
- Command enum which defines the PAGE PROGRAM command set (‘h00 – ‘h30)
- Row address which specifies LUN, BLOCK(PLANE) & PAGE address
- Column address which specifies the start address location inside the page
- Data size which defines the size of the data needs to be read from the page register.
- In case of status registers reading basing on the type status address fields can be ignored

The target memory and addressing layout defines the packet transaction fields which are shown as follows.

- **TARGET MEMORY ORGANIZATION**
- **ROW ADDRESS LAYOUT**

Tools & Technologies: Verilog, SystemVerilog, C, DPI, UVM
EDA Tools
Emulators

An ONFI transaction flow mainly follows 4 types of interface timing diagrams respective to each interface mode. The diagrams differ respective each interface among SDR, NV-DDR, NV-DDR2, and NV-DDR3.

→ Command latch timings
→ Address latch timings
→ Data input cycle timings
→ Data output cycle timings

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