OVERVIEW

Packet Generator is a software tool that will be running on a Host computer and generate traffic patterns.

PCIe packet generator is a product that generates series of Transaction Layer Packets (TLPs) which can be used by emulator platform to generate traffic on DUTs interfaces. Also, it can be used on Simulation platform to generate traffic on simulation environment on DUTs interface.

FEATURES

- It works on three types of configuration modes: Memory Packet, Configuration Packet and I/O Packet (for legacy devices).
- All PCIe Packet generation logic generates
  - 3DW header bits for Memory-Read (MRD) and Memory-Write (MWR) with 32-bit addressing, Config-Read (CFGRD), Config-Write (CFGWR), I/O-Read (IORD), I/O-Write (IOWR)
  - 4DW header bits for Memory-Read (MRD), Memory-Write (MWR) with 64-bit addressing
- The key aspects of the Transaction Layer are:
  - A pipelined full split-transaction protocol
  - Mechanisms for differentiating the ordering and processing requirements of TLPs
  - Credit-based flow control
  - Optional support for data poisoning and end-to-end data integrity detection
- The above TLPs generated will pass through Datalink Layer and then to Physical Layer to finally generate a serial data stream. Physical layer have 2 sub blocks named logical and physical sub block.
- The Data Link Layer is responsible for reliably conveying Transaction Layer Packets (TLPs) supplied by the Transaction Layer across a PCI Express Link to the other component's Transaction Layer. Services provided by the Data Link Layer include:
  - Data Exchange
  - Error Detection and Retry
  - Initialization and Power Management
- The logical sub-block has two main sections: a Transmit section that prepa res outgoing information passed from the Data Link Layer for transmission by the electrical sub -block, and a Receiver section that identifies and prepares received information before passing it to the Data Link Layer.
- PCI Express uses 8b/10b encoding when the data rate is 2.5 GT/s or 5.0 GT/s. For data rates greater than or equal to 8.0 GT/s, it uses a per-lane code along with physical layer encapsulation.

BENEFITS
• These methods can be used for verification of most complex hardware design to simple hardware design
• Easy to use solution, plug and play type solutions
• Software packet generators are very cost-effective solutions, they are cheaper compared to high license costing software products available in the market.
• Creates beautiful Emulation environment, which can mimic many simulation verification scenarios.
• Detect bug in Pre-silicon phase, which can save millions of dollars of re-spinning silicon cost.
• Post-silicon also software portion can be used for validation
• Help to build a parallel structure to simulation to find more design bugs quickly.
• The overall runtime can be reduced to as much as 10 times than long SOC simulations. This can speed up TAPE OUT of the chip.
• Scoreboarding and traffic analysis can be done very well in the Software solution.

CONFIGURATIONS

There are three configurations mode for packet generation:

- Memory Packet – Mode 1
  a. Memory Read (32-bit addressing) – Mode 11
  b. Memory Write (32-bit addressing) – Mode 12
  c. Memory Read (64-bit addressing) – Mode 13
  d. Memory Write (64-bit addressing) – Mode 14
- Configuration Packet – Mode 2
  a. Config Read – Mode 21
  b. Config Write – Mode 22
- I/O Packet – Mode 3
  a. I/O Read – Mode 31
  b. I/O Write – Mode 32

Memory Packet

Memory Packet comprises of both memory read and write with both 32 and 64 bit addressing header fields.
Memory packet format is as shown below,

- 32-bit addressing memory header
  It is a 3DW sized packet
- 64-bit addressing memory header
  It is a 4DW sized packet.

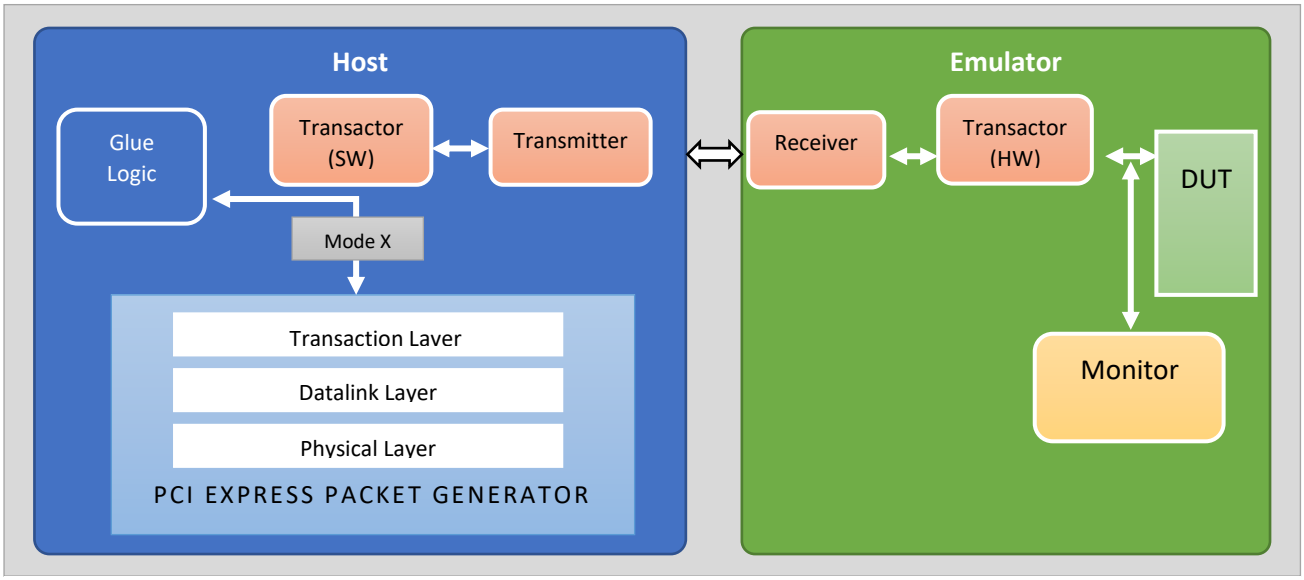

Figure 1: PCIe PACKET GENERATOR in EMULATION PLATFORM

Configuration Packet generation logic follows below rules

- Configuration Requests route by ID, and use a 3 DW header
- In addition to the header fields included in all Memory, I/O, and Configuration Requests and the ID routing fields, Configuration Requests contain the following additional fields
  - Register Number[5:0]
  - Extended Register Number[3:0]
- Configuration Requests have the following restrictions:
  - TC[2:0] must be 000b
  - LN is not applicable to Configuration Requests and the bit is Reserved
  - TH is not applicable to Configuration Requests and the bit is Reserved
  - Attr[2] is Reserved
  - Attr[1:0] must be 00b
  - AT[1:0] must be 00b. Receivers are not required or encouraged to check this
  - Length[9:0] must be 00 0000 0001b
  - Last DW BE[3:0] must be 0000b

Receivers may optionally check for violations of these rules (but must not check reserved bits). These checks are independently optional. If a Receiver implementing these checks determines that a TLP violates these rules, the TLP is a Malformed TLP. If checked, this is a reported error associated with the Receiving Port.

I/O Packet

I/O Packet generation logic follows below rules,

- I/O Requests route by address, using 32-bit Addressing
- I/O Requests have the following restrictions:
  - TC[2:0] must be 000b
  - LN is not applicable to I/O Requests and the bit is Reserved
  - TH is not applicable to I/O Request and the bit is Reserved Attr[2] is Reserved Attr[1:0] must be 00b
  - AT[1:0] must be 00b. Receivers are not required or encouraged to check this
  - Length[9:0] must be 00 0000 0001b
  - Last DW BE[3:0] must be 0000b

Receivers may optionally check for violations of these rules (but must not check reserved bits). These checks are independently optional. If a Receiver implementing these checks determines that a TLP violates these rules, the TLP is a Malformed TLP. If checked, this is a reported error associated with the Receiving Port.

Datalink Layer Packet Format

The packets generated from Transaction layer comes to Datalink layer which send then to receiver's datalink layer. Apart from the TLPs coming from upper layer, Datalink layer itself have its own packets for link managements.

The following DLLP Types are used to support Link operations:

- Ack DLLP: TLP Sequence number acknowledgement; used to indicate successful receipt of some number of TLPs
- Nak DLLP: TLP Sequence number negative acknowledgement; used to initiate a Data Link Layer Retry
- InitFC1, InitFC2, and UpdateFC DLLPs: For Flow Control
- DLLPs used for Power Management

Tools & Technologies: Verilog, SystemVerilog, C, DPI, UVM
EDA Tools
Emulators

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