OVERVIEW

Packet Generator is a software tool that will be running on a Host computer and generate traffic patterns.
MIPI CSI2 packet generator is a product that generates series of CSI2 packets which can be used by emulator platform to generate traffic on DUTs interfaces. It can also be used on Simulation platform to generate traffic on simulation environment on DUTs interface.

KEY FEATURES

- There are 2 types of packets: Long packet and short packet.
- It works with two types of phy: DPHY and CPHY.
- All MIPI CSI2 DPHY Long Packet generation logic includes
  - 32-bit Packet Header (PH), an application specific Data Payload with a variable number of 8-bit data words, and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count field and an 8-bit ECC. The Packet footer has one element, a 16-bit checksum (CRC).
- All MIPI CSI2 DPHY Short Packet generation logic includes
  - 32-bit Packet Header (PH) with no payload and no packet footer. The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit short packet data field and 8-bit ECC.
- All MIPI CSI2 CPHY Long Packet generation logic includes
  - four elements: a Packet Header (PH), an application specific Data Payload with a variable number of 8-bit data words, a 16-bit Packet Footer (PF), and zero or more Filler bytes (FILLER). The Packet Header is 6N x 16-bits long, where N is the number of C-PHY physical layer Lanes. The Packet Header consists of two identical 6N-byte halves, where each half consists of N sequential copies of each of the following fields: a 16-bit field containing eight Reserved bits plus the 8-bit Data Identifier (DI); the 16-bit Packet Data Word Count (WC); and a 16-bit Packet Header checksum (PH-CRC) which is computed over the previous four bytes. The value of each Reserved bit shall be zero. The Packet Footer consists of a 16-bit checksum (CRC) computed over the Packet Data using the same CRC polynomial as the Packet Header CRC and the Packet Footer used in the D-PHY physical layer option. Packet Filler bytes are inserted after the Packet Footer, if needed, to ensure that the Packet Footer ends on a 16-bit word boundary and that each C-PHY physical layer Lane transports the same number of 16-bit words (i.e. byte pairs).
- All MIPI CSI2 CPHY Short Packet generation logic includes
  - 6N*16-bit Packet Header (PH) with no payload and no packet footer. The Packet Header is further composed of four elements: an 8-bit Reserved bits, an 8-bit Data Identifier, a 16-bit short packet data field and 16-bit packet header CRC.
- The CSI2 packets are generated in the Protocol Layer which has 3 sub layers i.e

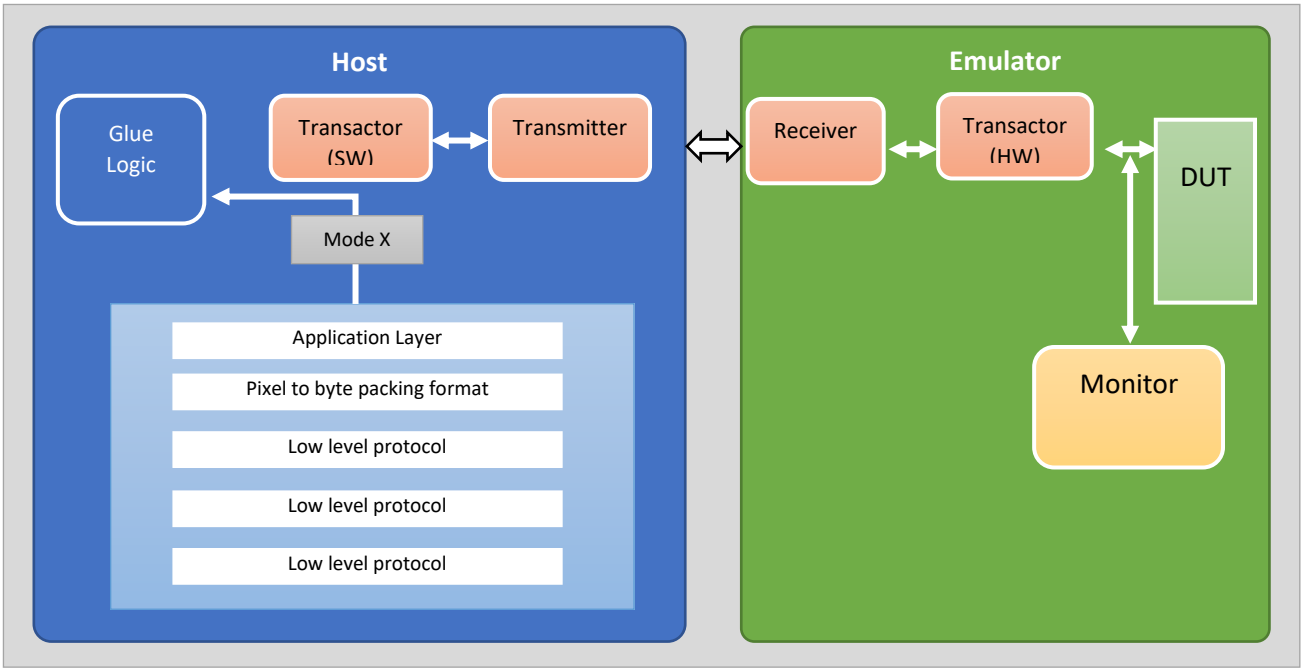

Figure 2: MIPI CSI2 PACKET GENERATOR in EMULATION PLATFORM

  - Pixels/Byte Packing/Unpacking Layer
  - Low Level Protocol
  - Lane Management Layer
- In Pixels/Byte Packing/Unpacking Layer, in transmitter this layer packs pixels from the Application layer into bytes before sending the data to the Low Level Protocol layer. In the receiver this layer unpacks bytes from the Low Level Protocol layer into pixels before sending the data to the 153 Application layer. Eight bits per pixel data is transferred unchanged by this layer.
- The Low Level Protocol (LLP) includes the means of establishing bit-155 level and byte-level synchronization for serial data transferred between SoT (Start of 156 Transmission) and EoT (End of Transmission) events and for passing data to the next layer. The 157 minimum data granularity of the LLP is one byte. The LLP also includes assignment of bit-value 158 interpretation within the byte, i.e. the "Endian" assignment.
- In Lane management, the transmitting side of the interface distributes ("distributor" function) bytes from the outgoing data stream to one or more Lanes. On the receiving side, the interface collects bytes from the Lanes and merges ("merger" function) them together into a recombined data stream that restores the original stream sequence. For the C-PHY physical layer option, this layer exclusively distributes or collects byte pairs (i.e. 16-bits) to or from the data Lanes.
- The phy layer specifies the transmission medium. There are two types of phy : DPHY and CPHY.
- The key aspects of the Low Level Protocol Layer are:
  - Transport of arbitrary data (Payload independent)
  - 8 bit word size
  - Support for up to 4 interleaved virtual channels (till v1.3) and 16 or 32 interleaved virtual channels (for v2.0 and above), respectively, on the same D-PHY or C-PHY link
  - Special packets for frame start, frame end, line start and line end information
  - Descriptor for the type, pixel depth and format of the Application Specific Payload data
  - 16-bit Checksum Code for error detection.
  - 8-bit Error Correction Code (till v1.3) and 6-bit Error Correction Code (for v2.0 and above) for error detection and correction (D-PHY physical layer only).

BENEFITS
• These methods can be used for verification of most complex hardware design to simple hardware design
• Easy to use solution, plug and play type solutions
• Software packet generators are very cost-effective solutions, they are cheaper compared to high license costing software products available in the market.
• Creates beautiful Emulation environment, which can mimic many simulation verification scenarios.
• Detect bug in Pre-silicon phase, which can save millions of dollars of re-spinning silicon cost.
• Post-silicon also software portion can be used for validation
• Help to build a parallel structure to simulation to find more design bugs quickly.
• The overall runtime can be reduced to as much as 10 times than long SOC simulations. This can speed up TAPE OUT of the chip.
• Scoreboarding and traffic analysis can be done very well in the Software solution.

LOW LEVEL PACKET FORMAT

There are 2 types of packets: Long packet and short packet.

Tools & Technologies:
Verilog, SystemVerilog, C, DPI, UVM
EDA Tools
Emulators

PHY TYPES

There are 2 phy types for packet generation:

- DPHY
  a. Long packet CSI2 versions below 2.0
  b. Short packet CSI2 versions below 2.0
  c. Long packet CSI2 versions equals or above 2.0
  d. Short packet CSI2 versions equals or above 2.0
- CPHY
  a. Long packet CSI2 versions below 2.0
  b. Short packet CSI2 versions below 2.0
  c. Long packet CSI2 versions equals or above 2.0
  d. Short packet CSI2 versions equals or above 2.0

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